A Linear Limiter : A 11-GHz Monolithic Low Distortion Variable Gain Amplifier

Masahiro Muraguchi and Masayoshi Aikawa

NTT Radio Communication Systems Laboratories
Yokosuka, Kanagawa 238-03 Japan

Abstract

A new 11-GHz monolithic low distortion variable gain amplifier is proposed. The amplifier maintains high lineality up to the high input power level using variable negative feedback. The third-order intermodulation distortion ratio of this amplifier is improved more than 40 dB compared with conventional variable gain amplifiers under compressed gain conditions.

I. Introduction

Digital radio systems require wide dynamic range and high linearity for receivers. The dynamic range of a receiver is limited at the low signal-level end by its noise figure performance and at the high signal-level end by its linearity as defined by the system requirements.

Figure 1 shows a receiver block diagram for an 11 GHz-band digital microwave system. The system requires more than 50 dB carrier-to-third-order intermodulation distortion ratio (IMR) for each amplifier over a very wide input power range from -75 dBm to -5 dBm. Moreover, the amplifier block also requires more than 20 dB total gain compression at a maximum input power of -5 dBm since the input power level of the mixer should be equal to or less than -15 dBm for linear operation.

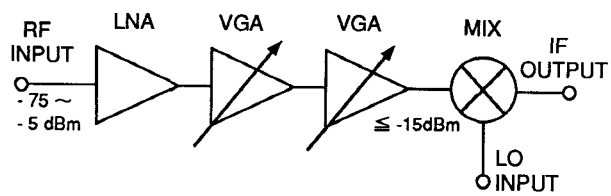

Fig. 1 Receiver block diagram for an 11 GHz-band digital microwave system.

Conventional variable gain FET amplifiers (VGAs) utilize the Vg or Vdd dependance of transconductance (gm). Cascode amplifiers and dual-gate FET amplifiers [1],[2], which are popular gain control amplifiers, belong to the drain-voltage controlled VGAs. The disadvantage of these types of VGAs is poor lineality under compressed gain conditions. This is why FET linearity degrades when the Vg or Vd is controlled to reduce the gm and gain. Furthermore, for the above system application, VGAs require considerable gain compression at a high input power level while the linearity of an FET becomes worse under such a large signal condition.

On the other hand, if an amplifier is composed of a variable attenuator and a small-signal amplifier unit, one can get rid of the above disadvantage. However, the dead loss or insertion loss of the attenuator in front of the amplifier unit directly degrades the noise figure of the amplifier. This results in a reduction of dynamic range because of the increase in low signal-level end.

II. New VGA configuration

In order to overcome the above problems, a new variable gain amplifier is proposed. The basic configuration of the amplifier is shown in Fig. 2 (a). The amplifier consists of an FET for amplification, an FET as a varistor, capacitors, fixed resistors, and matching networks. The amplifier employes a variable negative feedback configuration. It is known that negative feedback can significantly improve the linearity of amplifiers.[3] The gain can be changed by the control voltage (Vcont) of the FET varistor. When the varistor is controlled to a small resistance value, strong negative feedback occurs and the amplifier gain is compressed. Here, the RF signal amplitude at the FET gate terminal is reduced because

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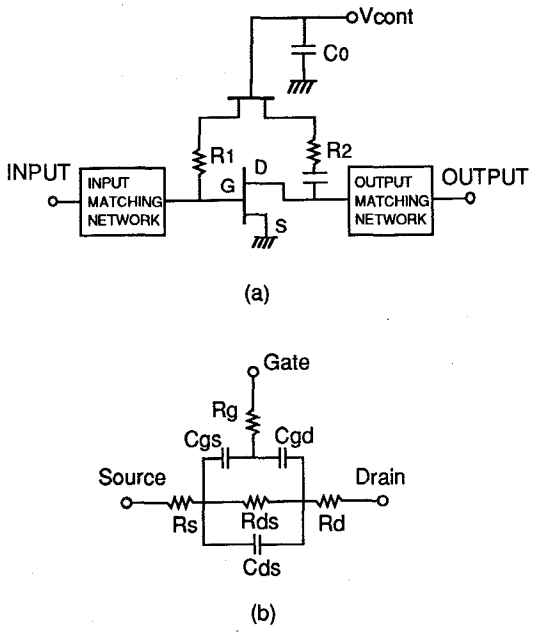

Fig. 2 (a) Proposed configuration for a low distortion variable gain FET amplifier.
(b) Equivalent circuit for an FET varistor.

the incident signal and feedback signal are combined in an out-of-phase manner at the FET gate terminal. This condition is considered equivalent to a small signal condition for the FET. Therefore, IMR improvement is expected under a compressed gain condition.

III. Circuit design

The equivalent circuit for the 11-GHz monolithic variable gain amplifier is shown in Fig. 3. The VGA uses two 0.3 μm x 240 μm-gate FETs for amplification and one 0.3 μm x 100 μm-gate FET as an FET varistor. An equivalent circuit of an FET varistor is shown in Fig. 2 (b). The FET varistor covers a resistance range from 30 Ω to 10k Ω. The parasitic capacitances Cgs and Cgd of the FET varistor make the VGA unstable, especially at a high varistor resistance. Therefore, the capacitor C0 and fixed resistors R1 and R2 are introduced to improve amplifier stability over the entire range of the Vcont. Here, C0 is employed as an RF grounding capacitor in order to eliminate the feedback through Cgs and Cgd when the resistance of Rds is high. In addition, a monolithic approach enhances the amplifier stability in spite of a considerably higher fre-

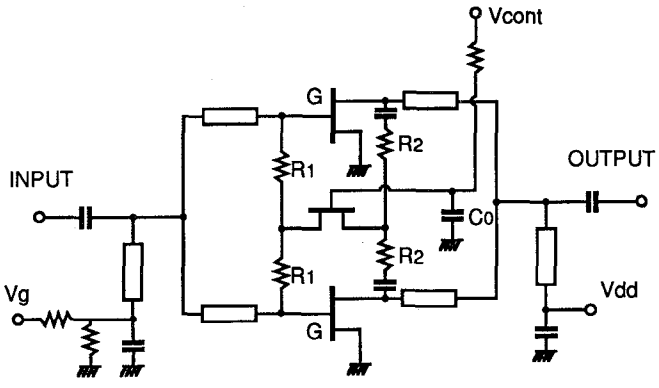

Fig. 3 Equivalent circuit for the 11-GHz monolithic low distortion variable gain amplifier.

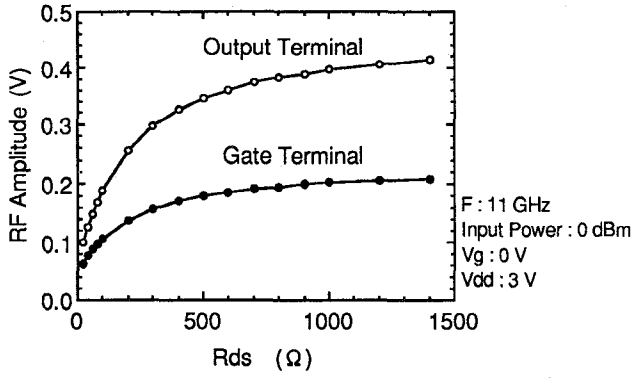

Fig. 4 Simulated RF amplitude at the output terminal and the gate terminals versus FET varistor resistance (Rds).

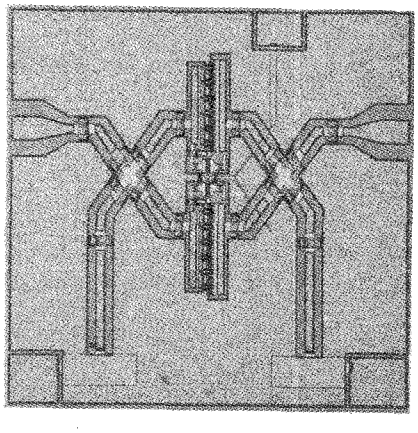

Fig. 5 Photograph of the monolithic VGA.
Chip size is 1.5 mm x 1.5 mm.

quency (11-GHz) since it can reduce the influence of parasitic parameters in the feedback circuit.

Figure 4 shows the simulated RF amplitude at the output terminal and the gate-terminal versus Rds. When Rds changes smaller, the RF amplitude at the gate-terminal as well as that at the output terminal is suppressed as expected. Since the RF amplitude at the gate-terminal is reduced to 1/3 at the low resistance end of the FET varistor, this corresponds to about 10 dB decrease in input power level.

IV. Measured Performance

The fabricated monolithic VGA is shown in Fig. 5. The dimensions of the chip are 1.5 x 1.5 mm. Coplanar waveguides are employed as transmission lines.

The measured output power versus input power for two control voltages (Vcont) for the FET varistor is shown in Fig. 6. Control voltages of -2.0 V and 0 V correspond to the high-end and low-end of the FET varistor resistance, respectively. The VGA has a maximum linear gain of 10 dB under Vcont of -2 V and a gain control range of 15 dB. The 1 dB gain compression point for Vcont of 0 V occurs at an input power of 11 dBm while that for Vcont of -2 V occurs at an input power of 0 dBm. The third-order intermodulation distortion ratio (IMR) versus input power for two Vcont values is shown in Fig. 7. The figure indicates more than 30 dB IMR improvement for a Vcont of 0 V at the same input power.

The measured fundamental output power per tone and IMR versus Vcont is shown in Fig. 8. The VGA has an IMR of 62 dB at a Vcont of 0 V with 14 dB gain compression. The figure indicates more than 35 dB IMR improvement by strong negative feedback. For reference, the measured fundamental output power per tone and IMR versus Vdd for an 11-GHz MMIC amplifier is shown in Fig. 9. The amplifier has an IMR of 18 dB at a Vdd of 0 V with 17 dB gain compression. This figure shows the unacceptable IMR degradation in the compressed gain region.

Figure 10 shows the measured gain and noise figure versus Vcont of the VGA. When the gain changes from 11 to -4 dB, the noise figure changes from 5.8 dB to 10 dB. The variation of noise figure is only 4.2 dB in spite of a gain variation of 15 dB. Therefore, this VGA surpasses the amplifier composed of a variable attenuator and a small-signal amplifier unit.

V. Conclusion

A new variable gain amplifier has been proposed. The third-order intermodulation distortion ratio of this VGA is improved more than 40 dB compared with conventional variable gain amplifiers under compressed gain conditions as shown in Figs. 8 and 9. The VGA maintains a high lineality up to the high input power level using variable negative feedback. Therefore, by adjusting the control voltage, the VGA can operate as a linear limiter up to a considerably higher input power level as shown in Fig.11. Here, the linear limiting power region will be extended by a cascade connection of the VGAs.

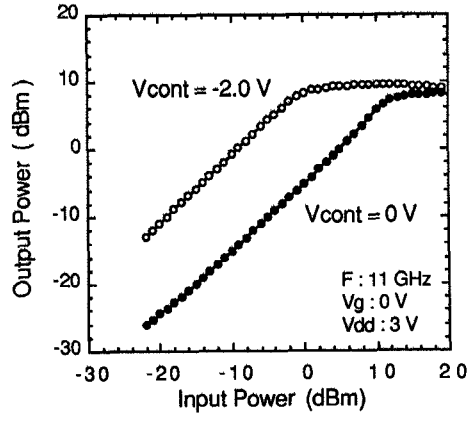

Fig. 6 Measured output power versus input power for the VGA.

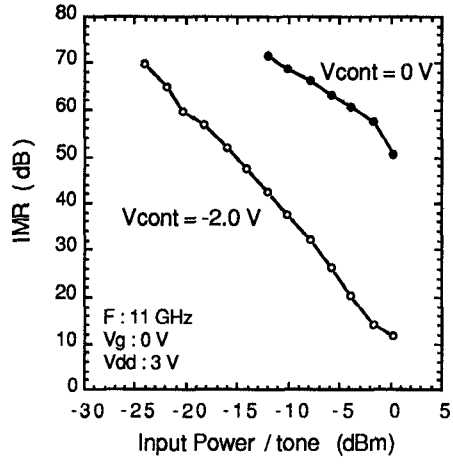

Fig. 7 Measured IMR versus input power (per tone) for the VGA. *(IMR: Carrier to third-order intermodulation distortion ratio)*

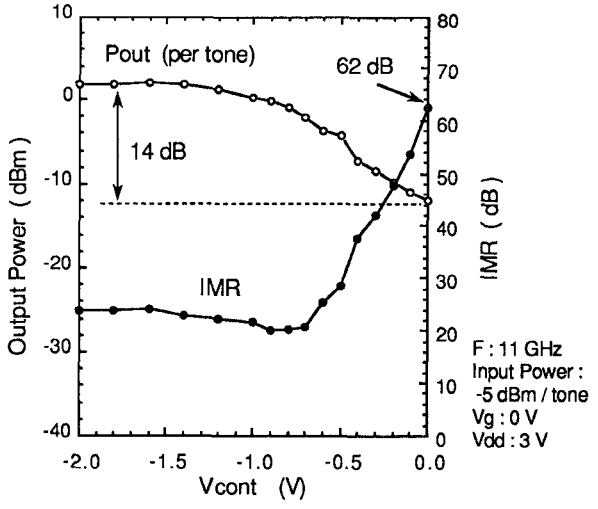

Fig. 8 Measured fundamental output power (per tone) and IMR versus Vcont for the VGA. *The figure indicates 62 dB IMR with 14 dB gain compression at Vcont of 0V.*

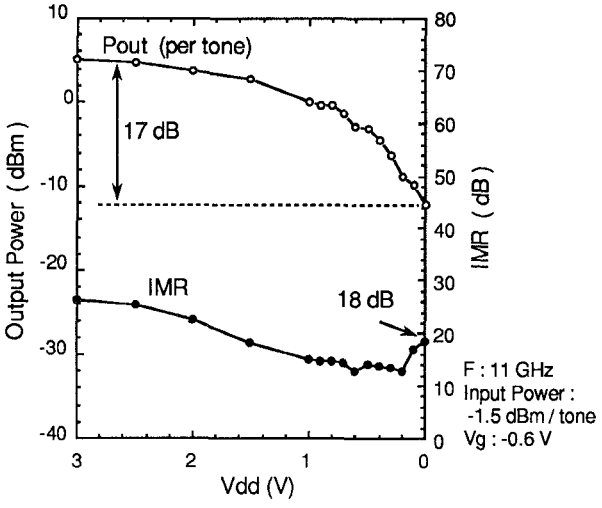

Fig. 9 Measured fundamental output power (per tone) and IMR versus Vdd for an 11-GHz MMIC amplifier. *The figure indicates 18 dB IMR with 17 dB gain compression at Vdd of 0V.*

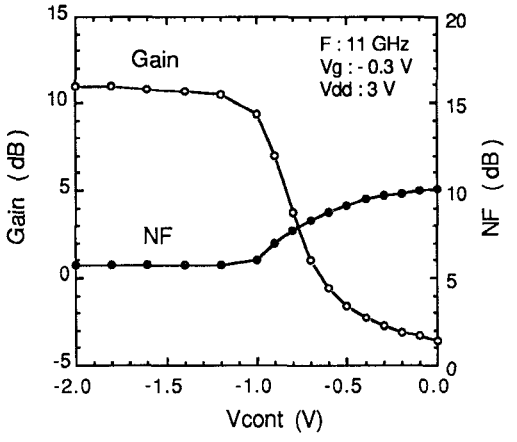

Fig. 10 Measured gain and noise figure versus Vcont for the VGA.

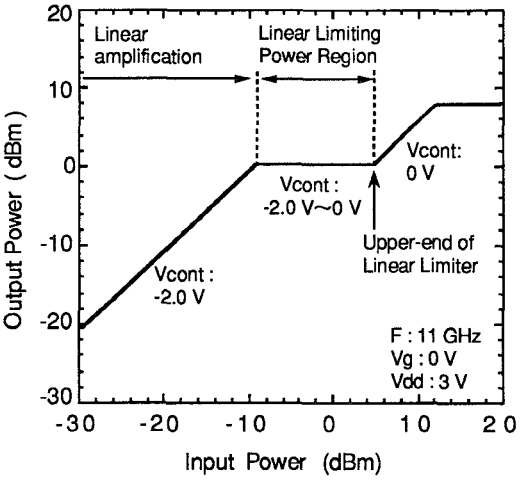

Fig. 11 Linear limiting power operation in the VGA. This limiter does not utilize the saturation region of the FET.

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